Refine Search

Search Results -

Terms	Documents
L3 or L4	25

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 13, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L5	l3 or l4	25	L5
L4	L2 and (programmable adj1 connector)	25	L4
L3	L2 same (programmable adj1 connector)	3	L3
L2	L1 near10 ("static random access memory" or SRAM)	930	L2
L1	"field programmable gate array" or FPGA	19042	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L5	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 13, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5	0	L6
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L5	l3 or l4	25	L5
L4	L2 and (programmable adj1 connector)	25	L4
L3	L2 same (programmable adj1 connector)	3	L3
L2	L1 near10 ("static random access memory" or SRAM)	930	L2
L1	"field programmable gate array" or FPGA	19042	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(365/185.01 |365/185.11 |716/16 |710/305 |710/100 |710/316 |710/300 |711/104 |326/37 |326/38 |326/39).ccls.	7884

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L7

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 13, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L7	710/305,100,316,300;326/37-39;365/185.01,185.11;711/104;716/16.ccls.	7884	L7
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5	0	L6
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L5	l3 or l4	25	L5
L4	L2 and (programmable adj1 connector)	25	L4
L3	L2 same (programmable adj1 connector)	3	L3
L2	L1 near10 ("static random access memory" or SRAM)	930	L2
L1	"field programmable gate array" or FPGA	19042	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L5 and L7	15

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L8

Refine Search

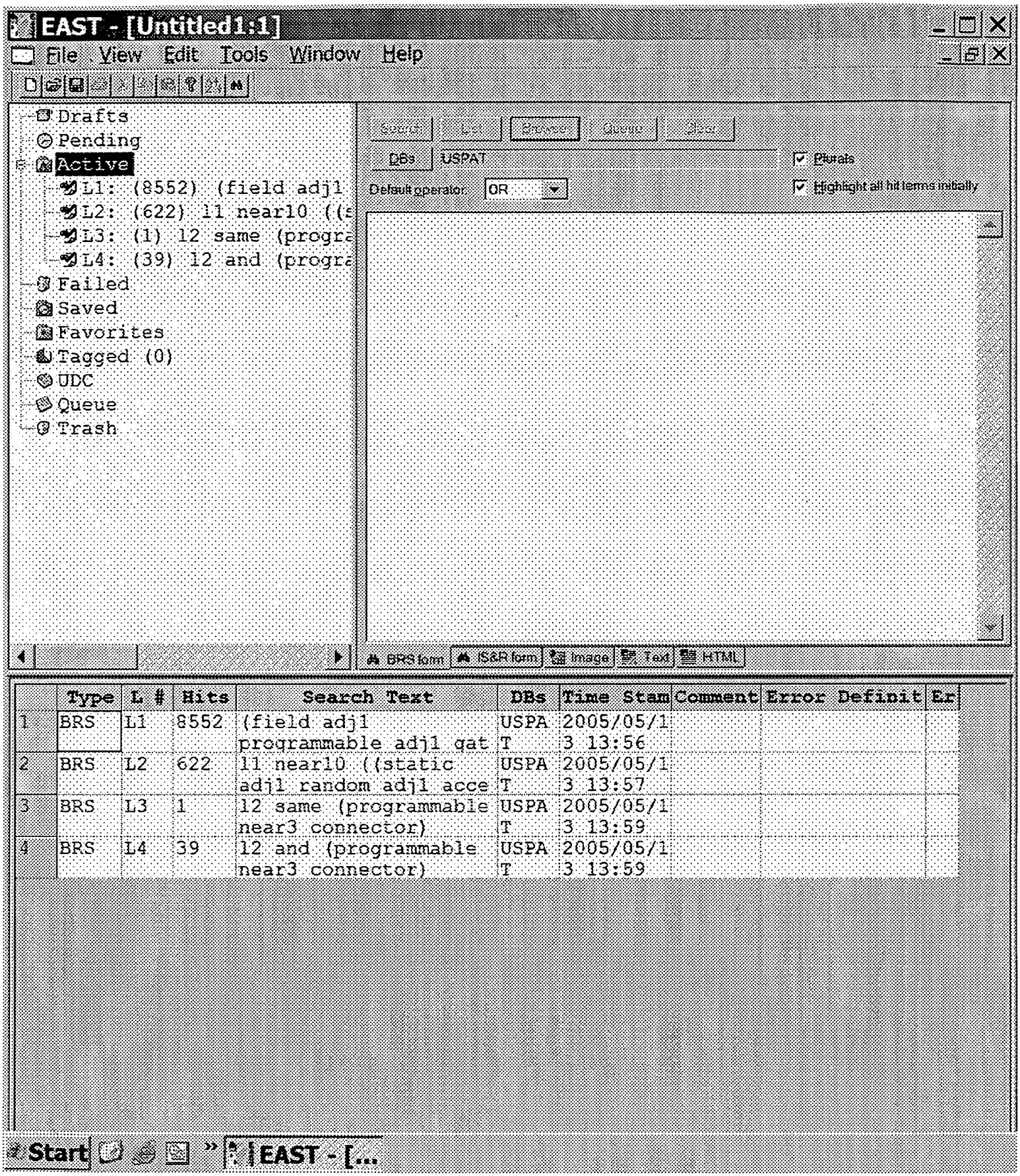
Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 13, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L8	l5 and L7	15	L8
L7	710/305,100,316,300;326/37-39;365/185.01,185.11;711/104;716/16.ccls.	7884	L7
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5	0	L6
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L5	l3 or l4	25	L5
L4	L2 and (programmable adj1 connector)	25	L4
L3	L2 same (programmable adj1 connector)	3	L3
L2	L1 near10 ("static random access memory" or SRAM)	930	L2
L1	"field programmable gate array" or FPGA	19042	L1

END OF SEARCH HISTORY


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
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L1: (8552) (field adj1
L2: (622) l1 near10 ((
L3: (1) l2 same (progra
L4: (39) l2 and (progra
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OR
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1 BRS L1 8552 (field adj1 programmable adj1 gat USPAT 2005/05/13 13:56
2 BRS L2 622 l1 near10 ((static adj1 random adj1 acce USPAT 2005/05/13 13:57
3 BRS L3 1 l2 same (programmable near3 connector) USPAT 2005/05/13 13:59
4 BRS L4 39 l2 and (programmable near3 connector) USPAT 2005/05/13 13:59
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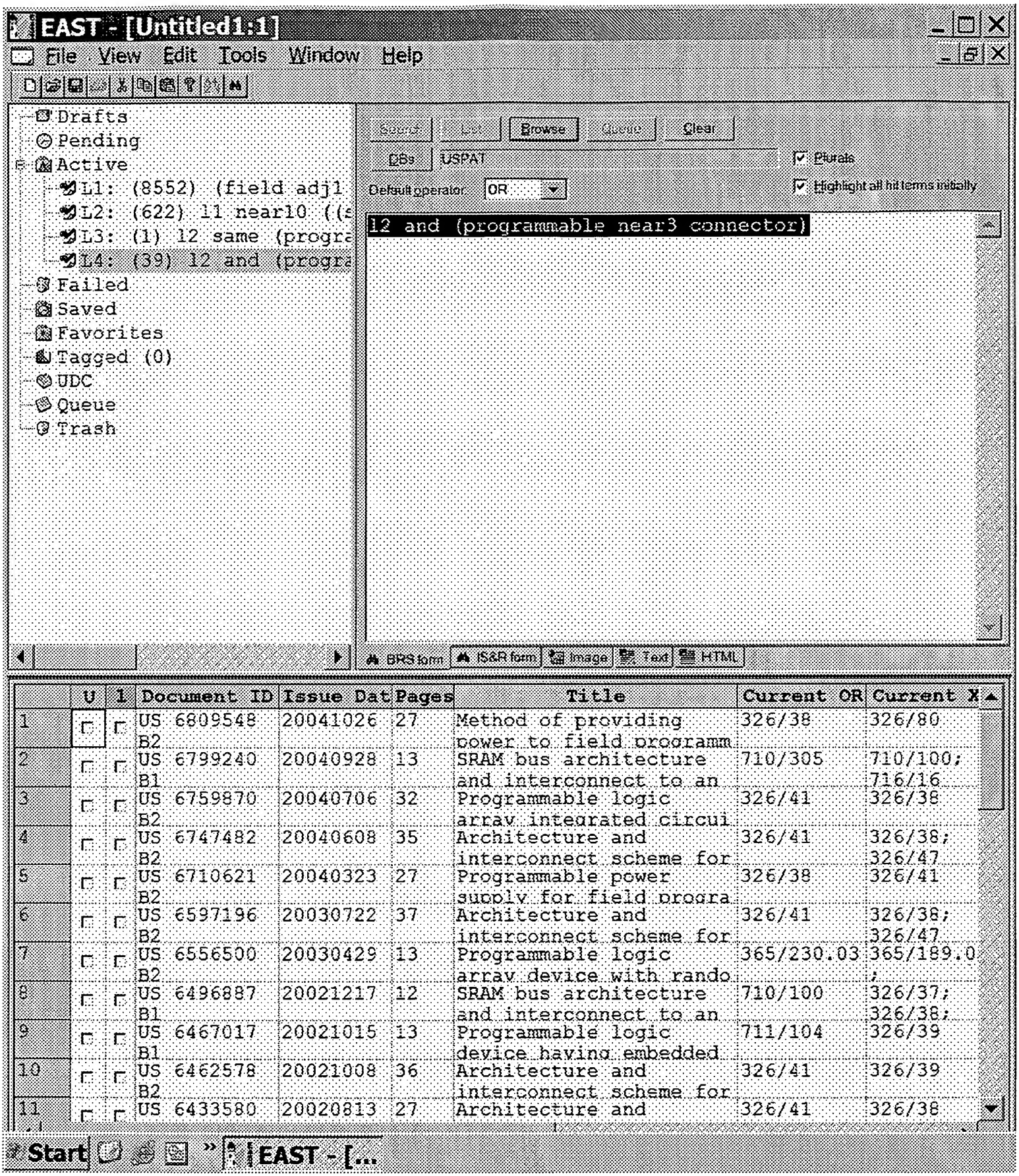
EAST - [...


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (8552) (field adj1
L2: (622) l1 near10 ((s
L3: (1) l2 same (progra
L4: (39) l2 and (progra
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USPAT
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OR
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l2 and (programmable near3 connector)
BRS form
IS&R form
Image
Text
HTML
U
1
Document ID
Issue Dat
Pages
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Current OR
Current X
1 US 6809548 B2 20041026 27 Method of providing power to field programm 326/38 326/80
2 US 6799240 B1 20040928 13 SRAM bus architecture and interconnect to an 710/305 710/100; 716/16
3 US 6759870 B2 20040706 32 Programmable logic array integrated circui 326/41 326/38
4 US 6747482 B2 20040608 35 Architecture and interconnect scheme for 326/41 326/38; 326/47
5 US 6710621 B2 20040323 27 Programmable power supply for field progra 326/38 326/41
6 US 6597196 B2 20030722 37 Architecture and interconnect scheme for 326/41 326/38; 326/47
7 US 6556500 B2 20030429 13 Programmable logic array device with rando 365/230.03 365/189.0 ;
8 US 6496887 B1 20021217 12 SRAM bus architecture and interconnect to an 710/100 326/37; 326/38;
9 US 6467017 B1 20021015 13 Programmable logic device having embedded 711/104 326/39
10 US 6462578 B2 20021008 36 Architecture and interconnect scheme for 326/41 326/39
11 US 6433580 20020813 27 Architecture and 326/41 326/38
Start
EAST - [...

Results for "(field programmable gate array<in>metadata) <and> (static random access memory<in..."

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(field programmable gate array<in>metadata) <and> (static random access memor >>

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Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **VHDL modeling and simulation of the back-propagation algorithm and its mapping to the RM**
Erdogan, S.S.; Wahab, A.; Hong, T.H.;
Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993
9-12 May 1993 Page(s):3.3.1 - 3.3.4
AbstractPlus | Full Text: PDF(348 KB) IEEE CNF

2. **Intel's FLEXlogic FPGA architecture**
Smith, D.E.;
Compcon Spring '93, Digest of Papers.
22-26 Feb. 1993 Page(s):378 - 384
AbstractPlus | Full Text: PDF(320 KB) IEEE CNF

3. **Field programmable gate arrays**
Verma, H.;
Potentials, IEEE
Volume 18, Issue 4, Oct.-Nov. 1999 Page(s):34 - 36
AbstractPlus | Full Text: PDF(424 KB) IEEE JNL

4. **FPGAs widen the ARGO-YBJ experiment's eyes**
Aloisio, A.; Branchini, P.; Cavaliere, S.; Parascandolo, P.;
Nuclear Science, IEEE Transactions on
Volume 49, Issue 2, April 2002 Page(s):401 - 404
AbstractPlus | References | Full Text: PDF(358 KB) IEEE JNL

5. **SRAM based re-programmable FPGA for space applications**
Wang, J.J.; Katz, R.B.; Sun, J.S.; Cronquist, B.E.; McCollum, J.L.; Speers, T.M.; Plants, W.C.;
Nuclear Science, IEEE Transactions on
Volume 46, Issue 6, Dec. 1999 Page(s):1728 - 1735
AbstractPlus | Full Text: PDF(448 KB) IEEE JNL

6. **Partial-encryption technique for intellectual property protection of FPGA-based products**
Kun-Wah Yip; Tung-Sang Ng;
Consumer Electronics, IEEE Transactions on
Volume 46, Issue 1, Feb. 2000 Page(s):183 - 190
AbstractPlus | Full Text: PDF(364 KB) IEEE JNL

7. **The design of a SRAM-based field-programmable gate array-Part II: Circuit design and layout**
Chow, P.; Soon Ong Seo; Rose, J.; Chung, K.; Paez-Monzon, G.; Rahardja, I.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 7, Issue 3, Sept. 1999 Page(s):321 - 330

AbstractPlus | References | Full Text: PDF(524 KB) IEEE JNL

8. **The design of an SRAM-based field-programmable gate array. I. Architecture**
Chow, P.; Soon Ong Seo; Rose, J.; Chung, K.; Paez-Monzon, G.; Rahardja, I.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 7, Issue 2, June 1999 Page(s):191 - 197

AbstractPlus | References | Full Text: PDF(180 KB) IEEE JNL

9. **A reconfigurable signal processing IC with embedded FPGA and multiport Flash memory**
Borgatti, M.; Cali, L.; De Sandre, G.; Foret, B.; Lertora, I.F.; Muzzi, G.; Pasotti, M.; Poles, M.; Rolandi, P.L.;
Design Automation Conference, 2003. Proceedings
2-6 June 2003 Page(s):691 - 695

AbstractPlus | Full Text: PDF(509 KB) IEEE CNF

SRAM based re-programmable FPGA for space applications

Wang, J.J. Katz, R.B. Sun, J.S. Cronquist, B.E. McCollum, J.L. Speers, T.M. Plants, W.C.
Actel Corp., Sunnyvale, CA, USA;

This paper appears in: **Nuclear Science, IEEE Transactions on**
Publication Date: Dec. 1999
Volume: 46 , Issue: 6
On page(s): 1728 - 1735
Meeting Date: 07/12/1999 - 07/16/1999
Location: Norfolk, VA
ISSN: 0018-9499
CODEN: IETNAE
INSPEC Accession Number:6501195
DOI: 10.1109/23.819146
Posted online: 2002-08-06 22:51:08.0

Abstract
An SRAM (**static random access memory**)-based reprogrammable FPGA (**field programmable gate array**) is investigated for space applications. A new commercial prototype, named the RS family, was used as an example for the investigation. The device is fabricated in a 0.25 μm CMOS technology. Its architecture is reviewed to provide a better understanding of the impact of single event upset (SEU) on the device during operation. The SEU effect of different memories available on the device is evaluated. Heavy ion test data and SPICE simulations are used integrally to extract the threshold LET (linear energy transfer). Together with the saturation cross-section measurement from the layout, a rate prediction is done on each memory type. The SEU in the configuration SRAM is identified as the dominant failure mode and is discussed in detail. The single event transient error in combinational logic is also investigated and simulated by SPICE. SEU mitigation by hardening the memories and employing EDAC (error detection and correction) at the device level are presented. For the configuration SRAM (CSRAM) cell, the trade-off between resistor dc-coupling and redundancy hardening techniques are investigated with interesting results. Preliminary heavy ion test data show no sign of SEL (single event latch-up). With regard to ionizing radiation effects, the increase in static leakage current (static I_{CC}) measured indicates a device tolerance of approximately 50 krad(Si)

Index Terms
Inspec

Controlled Indexing
CMOS logic circuits CMOS memory circuits SPICE SRAM chips aerospace instrumentation failure analysis **field programmable gate arrays** integrated circuit measurement integrated circuit reliability integrated circuit testing ion beam effects radiation hardening (electronics)

Non-controlled Indexing
0.25 mum 50 krad CMOS technology CSRAM EDAC RS SRAM SPICE simulations SRAM based re-programmable FPGA architecture combinational logic configuration SRAM device tolerance error detection and correction failure mode **field programmable gate array** hardening heavy ion test data ionizing radiation effects

linear energy transfer rate prediction redundancy hardening techniques resistor dc-coupling saturation cross-section single event latch-up single event transient error single event upset space applications static leakage current static random access memory threshold LET

Author Keywords

Not Available

References

No references available on IEEE Xplore.

Citing Documents

1 Proton radiation effects in XC4036XLA field programmable gate arrays, Buchanan, N.J.; Gingrich, D.M.
Nuclear Science, IEEE Transactions on
On page(s): 263- 271, Volume: 50, Issue: 2, Apr 2003
Abstract | Full Text: PDF (405)

2 Single event upset and hardening in 0.15 /spl mu/m antifuse-based field programmable gate array, Wang, J.J.; Wong, W.; Wolday, S.; Cronquist, B.; McCollum, J.; Katz, R.; Kleyner, I.
Nuclear Science, IEEE Transactions on
On page(s): 2158- 2166, Volume: 50, Issue: 6, Dec. 2003
Abstract | Full Text: PDF (611)

3 A review of ionizing radiation effects in floating gate memories, Cellere, G.; Paccagnella, A.
Device and Materials Reliability, IEEE Transactions on
On page(s): 359- 370, Volume: 4, Issue: 3, Sept. 2004
Abstract | Full Text: PDF (768)

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Intel's FLEXlogic FPGA architecture

Smith, D.E.
Intel Corp., Folsom, CA, USA;

This paper appears in: **Compcon Spring '93, Digest of Papers.**
Publication Date: 22-26 Feb. 1993
On page(s): 378 - 384
Meeting Date: 02/22/1993 - 02/26/1993
Location: San Francisco, CA
INSPEC Accession Number:4750287
DOI: 10.1109/CMPCON.1993.289700
Posted online: 2002-08-06 18:51:47.0

Abstract
Intel's FLEXlogic **field-programmable gate array** family is a segmented architecture, SRAM (**static random-access memory**)-based family with on-chip nonvolatile memory. The architecture is quick to learn and easy to use for designers with standard PLD experience. Devices are organized into configurable function blocks (CFBs). Each CFB can be configured as a PLD block or as a bank of SRAMs. CFBs configured as PLD blocks include advanced features that provide significant design flexibility and high integration. Truly predictable timing simplifies the design and simulation process. The inherent speed of the FLEXlogic FPGA family, together with its selectable 3.3-V or 5-V I/O, allows it to be used in areas where previous FPGA architectures cannot operate. The iFX780, the first member of the family, illustrates the architecture

Index Terms
Inspec

Controlled Indexing

3.3 V 5.5 V FPGA architecture Intel FLEXlogic PLD blocks SRAM SRAM chips computer architecture configurable function blocks design flexibility **field-programmable gate array** high integration iFX780 logic arrays on-chip nonvolatile memory predictable timing segmented architecture selectable I/O voltage simulation process **static random-access memory**

Non-controlled Indexing

3.3 V 5.5 V FPGA architecture Intel FLEXlogic PLD blocks SRAM SRAM chips computer architecture configurable function blocks design flexibility **field-programmable gate array** high integration iFX780 logic arrays on-chip nonvolatile memory predictable timing segmented architecture selectable I/O voltage simulation process **static random-access memory**

Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

1 The design of an SRAM-based field-programmable gate array. I. Architecture, Chow, P.; Soon Ong Seo; Rose, J.; Chung, K.; Paez-Monzon, G.; Rahardja, I.
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
On page(s): 191-197, Volume: 7, Issue: 2, Jun 1999
Abstract | Full Text: PDF (180)

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Search Results - Record(s) 1 through 10 of 25 returned.

1. Document ID: US 20040199689 A1

L5: Entry 1 of 25 File: PGPB Oct 7, 2004

PGPUB-DOCUMENT-NUMBER: 20040199689
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040199689 A1

TITLE: SRAM bus architecture and interconnect to an FPGA

PUBLICATION-DATE: October 7, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Plants, William C.	Santa Clara	CA	US	

US-CL-CURRENT: 710/100

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

2. Document ID: US 20040024799 A1

L5: Entry 2 of 25 File: PGPB Feb 5, 2004

PGPUB-DOCUMENT-NUMBER: 20040024799
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040024799 A1

TITLE: General-purpose functional circuit and general-purpose unit for programmable controller

PUBLICATION-DATE: February 5, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ohno, Koji	Osaka		JP	
Noda, Hideki	Osaka		JP	
Mishina, Kazuhiro	Shiga		JP	

US-CL-CURRENT: 708/139

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

3. Document ID: US 20030151426 A1

L5: Entry 3 of 25 File: PGPB Aug 14, 2003

PGPUB-DOCUMENT-NUMBER: 20030151426
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030151426 A1

TITLE: Logic circuits using polycrystalline semiconductor thin film transistors

PUBLICATION-DATE: August 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Islam, Mujahid	Cambridge		GB	

US-CL-CURRENT: 326/37

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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☐ 4. Document ID: US 6799240 B1

L5: Entry 4 of 25 File: USPT Sep 28, 2004

US-PAT-NO: 6799240
DOCUMENT-IDENTIFIER: US 6799240 B1

TITLE: SRAM bus architecture and interconnect to an FPGA

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

---

☐ 5. Document ID: US 6759870 B2

L5: Entry 5 of 25 File: USPT Jul 6, 2004

US-PAT-NO: 6759870
DOCUMENT-IDENTIFIER: US 6759870 B2

TITLE: Programmable logic array integrated circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6417690 B1

L5: Entry 6 of 25 File: USPT Jul 9, 2002

US-PAT-NO: 6417690
DOCUMENT-IDENTIFIER: US 6417690 B1
** See image for Certificate of Correction **

TITLE: Floor plan for scalable multiple level tab oriented interconnect architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 6404225 B1

L5: Entry 7 of 25 File: USPT Jun 11, 2002

US-PAT-NO: 6404225
DOCUMENT-IDENTIFIER: US 6404225 B1

TITLE: Integrated circuit incorporating a programmable cross-bar switch

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 6362646 B1

L5: Entry 8 of 25 File: USPT Mar 26, 2002

US-PAT-NO: 6362646
DOCUMENT-IDENTIFIER: US 6362646 B1

TITLE: Method and apparatus for reducing memory resources in a programmable logic device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 6326807 B1

L5: Entry 9 of 25 File: USPT Dec 4, 2001

US-PAT-NO: 6326807
DOCUMENT-IDENTIFIER: US 6326807 B1

TITLE: Programmable logic architecture incorporating a content addressable embedded array block

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 10. Document ID: US 6300793 B1

L5: Entry 10 of 25 File: USPT Oct 9, 2001

US-PAT-NO: 6300793
DOCUMENT-IDENTIFIER: US 6300793 B1

TITLE: Scalable multiple level tab oriented interconnect architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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Terms	Documents
L3 or L4	25

Display Format: - Change Format

Previous Page Next Page Go to Doc#

L5: Entry 9 of 25 File: USPT Dec 4, 2001

US-PAT-NO: 6326807
DOCUMENT-IDENTIFIER: US 6326807 B1

TITLE: Programmable logic architecture incorporating a content addressable embedded array block

DATE-ISSUED: December 4, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Veenstra; Kerry	San Jose	CA		
Heile; Francis B.	Santa Clara	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Altera Corporation	San Jose	CA			02

APPL-NO: 09/ 689269 [PALM]
DATE FILED: October 11, 2000

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATION This application is a Continuation application of prior application Ser. No. 09/167,220 filed on Oct. 6, 1998 now U.S. Pat. No. 6,160,419 and entitled "PROGRAMMABLE LOGIC ARCHITECTURE INCORPORATING A CONTENT ADDRESSABLE EMBEDDED ARRAY BLOCK, the disclosure of which is incorporated herein by reference. This application is also a continuation-in-part of U.S. application Ser. No. 09/034,050 filed Mar. 3, 1998 now U.S. Pat. No. 6,020,759 and entitled "PROGRAMMABLE LOGIC ARRAY DEVICE WITH RANDOM ACCESS MEMORY CONFIGURABLE AS PRODUCT TERMS" which is hereby incorporated by reference. This application also claims benefit of priority under 35 U.S.C. .sctn.119(e) of U.S. Provisional Application No. 60/064054, filed Nov. 3, 1997, and entitled "PROGRAMMABLE LOGIC ARCHITECTURE INCORPORATING A CONTENT ADDRESSABLE EMBEDDED ARRAY BLOCK" which is hereby incorporated by reference, which claim benefit to Provisional Application No. 60/041,046 filed Mar. 21, 1997.

INT-CL: [07] H01 L 25/00

US-CL-ISSUED: 326/40; 326/41, 326/39, 326/38
US-CL-CURRENT: 326/40; 326/38, 326/39, 326/41

FIELD-OF-SEARCH: 326/37-41, 365/189.05, 365/189.08

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3849638	November 1974	Greer	
☐	4740917	April 1988	Denis et al.	

☐	4876466	October 1989	Kondou et al.	
☐	5099150	March 1992	Steele	
☐	5270587	December 1993	Zagar	
☐	5383146	January 1995	Threewitt	
☐	5408434	April 1995	Stansfield	
☐	5473267	December 1995	Stansfield	
☐	5532957	July 1996	Malhi	
☐	5550782	August 1996	Cliff et al.	
☐	5557218	September 1996	Jang	
☐	5559450	September 1996	Ngai et al.	
☐	5559747	September 1996	Kasamizugami et al.	
☐	5804986	September 1998	Jones	326/40
☐	5809281	September 1998	Steele et al.	
☐	5943252	August 1999	Schultz et al.	365/49
☐	6041388	March 2000	Anumula et al.	365/49
☐	6114873	September 2000	Sahraoui et al.	326/39
☐	6148364	November 2000	Srinivasan et al.	711/108

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 612 154	August 1994	EP	

OTHER PUBLICATIONS

Stansfield, Anthony and Page, Ian. "The Design of a New FPGA Architecture", FPL, 1995.
Barre, "Using FPLA's: Evaluating the applications of a powerful component which can show itself to be very economical", Electronique et applications Industrielles, Apr. 1, 1978.
Kaviani et al., "Hybrid FPGA Architecture", Proceedings 4.sup.th International Symposium on FPGA's (FPGA 96), Feb. 1996.
Press release, "Altera Enables System-Level Integration With Rafael Family of Embedded PLDs", Aug. 31, 1998, http://www.altera.com/html/new/pressrel/pr_rafael12.html.
Press release, "Altera Unveils New Name for Rafael: Advanced Programmable Embedded Matrix (APEX)", Aug. 31, 1998, http://www.altera.com/html/new/pressrel/pr_apex1.html.
Datasheet, "Apex 20K Device Family: Breakthrough MultiCore Architecture", http://www.altera.com/html/products/apex2.html.
Datasheet, "Apex 20K Device Family: The Embedded PLD Family for System-Level Integration", http://www.altera.com/html/products/apex.html.
Bursky, Dave, "Combination RAM/PLD Opens New Application Options", Electronic Design, pp. 138-140, May 23, 1991.
Intel Corporation "10 ns FLEXlogic FPGA with SRAM Option", INTEL.RTM..sup., iFX780, pp. 2-24--2-46, Nov. 1993.
Ngai, Tony Kai-Kit, "An SRAM-Programmable Field-Reconfigurable Memory",Department of Electrical Engineering, University of Toronto, Thesis for Master of Applied Science, 1994.
Brown et al., "FPGA and CPLD Architectures: A Tutorial", vol. 13, No. 2, pp. 42-57, Jun. 1, 1996, IEEE Design and Test of Computers.
Reddy et al., "A High Density Embedded Array Programmable Logic Architecture", May 5-8, 1996, Proceedings of the IEEE 1996 Custom Integrated Circuits Conference, San Diego.
"Embedded Memory Enhances Programmable Logic for Complex, Compact Designs", Nov. 7, 1996, vol. 41, No. 23, EDN Electrical Design News.
Altera corporation "APEX 20k Programmable Logic Device Family", ALTERA.RTM. Oct. 1998, ver.1.

ART-UNIT: 289

PRIMARY-EXAMINER: Tokar; Michael

ASSISTANT-EXAMINER: Tan; Vibol

ATTY-AGENT-FIRM: Beyer Weaver & Thomas LLP

ABSTRACT:

The invention relates to an integrated circuit that can be configured to operate as a content addressable memory. The integrated circuit includes a first functional block that stores at least one keyword dataword which is associated with a group of associated data words. The integrated circuit also includes a second functional block that stores the group of associated datawords. The second functional block is connected to the first functional block in such a way that if a request dataword received at the first functional block matches at least one keyword dataword stored therein, then an associated result dataword included in the group of associated data words stored in the second functional block is output by the second functional block. Typically, the integrated circuit chip is a complex programmable logic device architecture (CPLD).

13 Claims, 9 Drawing figures

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Search Results - Record(s) 11 through 20 of 25 returned.

☐ 11. Document ID: US 6292017 B1

L5: Entry 11 of 25 File: USPT Sep 18, 2001

US-PAT-NO: 6292017
DOCUMENT-IDENTIFIER: US 6292017 B1

TITLE: Programmable logic device incorporating function blocks operable as wide-shallow RAM

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 12. Document ID: US 6249143 B1

L5: Entry 12 of 25 File: USPT Jun 19, 2001

US-PAT-NO: 6249143
DOCUMENT-IDENTIFIER: US 6249143 B1

TITLE: Programmable logic array integrated circuit with distributed random access memory array

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 13. Document ID: US 6195788 B1

L5: Entry 13 of 25 File: USPT Feb 27, 2001

US-PAT-NO: 6195788
DOCUMENT-IDENTIFIER: US 6195788 B1

TITLE: Mapping heterogeneous logic elements in a programmable logic device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 14. Document ID: US 6181159 B1

L5: Entry 14 of 25 File: USPT Jan 30, 2001

US-PAT-NO: 6181159
DOCUMENT-IDENTIFIER: US 6181159 B1

TITLE: Integrated circuit incorporating a programmable cross-bar switch

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 15. Document ID: US 6160419 A

L5: Entry 15 of 25 File: USPT Dec 12, 2000

US-PAT-NO: 6160419
DOCUMENT-IDENTIFIER: US 6160419 A

TITLE: Programmable logic architecture incorporating a content addressable embedded array block

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

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☐ 16. Document ID: US 6134173 A

L5: Entry 16 of 25 File: USPT Oct 17, 2000

US-PAT-NO: 6134173
DOCUMENT-IDENTIFIER: US 6134173 A
** See image for Certificate of Correction **

TITLE: Programmable logic array integrated circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

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☐ 17. Document ID: US 6104208 A

L5: Entry 17 of 25 File: USPT Aug 15, 2000

US-PAT-NO: 6104208
DOCUMENT-IDENTIFIER: US 6104208 A

TITLE: Programmable logic device incorporating function blocks operable as wide-shallow RAM

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

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☐ 18. Document ID: US 6064599 A

L5: Entry 18 of 25 File: USPT May 16, 2000

US-PAT-NO: 6064599
DOCUMENT-IDENTIFIER: US 6064599 A
** See image for Certificate of Correction **

TITLE: Programmable logic array integrated circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw. Desc | Image

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☐ 19. Document ID: US 6057707 A

L5: Entry 19 of 25 File: USPT May 2, 2000

US-PAT-NO: 6057707
DOCUMENT-IDENTIFIER: US 6057707 A

TITLE: Programmable logic device incorporating a memory efficient interconnection device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw Desc | Image

20. Document ID: US 6038627 A

L5: Entry 20 of 25 File: USPT Mar 14, 2000

US-PAT-NO: 6038627
DOCUMENT-IDENTIFIER: US 6038627 A

TITLE: SRAM bus architecture and interconnect to an FPGA

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw Desc | Image

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Terms	Documents
L3 or L4	25

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L5: Entry 12 of 25 File: USPT Jun 19, 2001

US-PAT-NO: 6249143
DOCUMENT-IDENTIFIER: US 6249143 B1

TITLE: Programmable logic array integrated circuit with distributed random access memory array

DATE-ISSUED: June 19, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Zaveri; Ketan	San Jose	CA		
Cliff; Richard	Milpitas	CA		
Reddy; Srinivas	Santa Clara	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Altera Corporation	San Jose	CA			02

APPL-NO: 09/ 007718 [PALM]
DATE FILED: January 15, 1998

PARENT-CASE:
This application is a regular U.S. patent application of U.S. provisional application Ser. No. 60/047,625 filed May 23, 1997.

INT-CL: [07] G06 F 7/38, H03 K 19/177

US-CL-ISSUED: 326/40; 326/39
US-CL-CURRENT: 326/40; 326/39

FIELD-OF-SEARCH: 326/39, 326/40, 326/41, 326/47, 326/38

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4706216	November 1987	Carter	
☐	4780846	October 1988	Tanabe et al.	365/63
☐	4870302	September 1989	Freeman	
☐	5274581	December 1993	Cliff et al.	
☐	5343406	August 1994	Freeman et al.	
☐	5352940	October 1994	Watson	
☐	5386154	January 1995	Goetting et al.	

☐	5414377	May 1995	Freidin	
☐	5481486	January 1996	Cliff et al.	
☐	5550782	August 1996	Cliff et al.	365/230.03
☐	5566123	October 1996	Freidin et al.	
☐	5570040	October 1996	Lytle et al.	
☐	5572148	November 1996	Lytle et al.	326/41
☐	5581198	December 1996	Trimberger	
☐	5644251	July 1997	Colwell et al.	326/16
☐	5689195	November 1997	Cliff et al.	326/41
☐	5705938	January 1998	Kean	326/39
☐	5744980	April 1998	McGowan et al.	326/40

OTHER PUBLICATIONS

Actel, "Actel's Reprogrammable SPGAs," Actel Corporation, Preliminary Advance Information (Oct. 10, 1996), pp. 1, 8-9.
AT&T Microelectronics, "ORCA FPGAs Excel in Multiplexing and On-Chip SRAM Applications," (Article Reprinted from App Review, Apr. 11, 1994), Application Note (Dec. 1995), pp. 1-4.
Bursky, Dave, "Programmable Arrays Mix FPGA And ASIC Blocks," Electronic Design, pp. 69-74, (Oct. 14, 1996).
Ngai, T, et al., "A New Generation of ORCA FPGA with Enhanced Features and Performance," IEEE 1996 Custom Integrated Circuits Conference, pp. 247-250.
Xilinx, Inc., "XC4000 Series Field Programmable Gate Arrays," Product Specification, V. 1.04, pp. 4-5-4-24 (Sep. 18, 1996).

ART-UNIT: 289

PRIMARY-EXAMINER: Tokar; Michael

ASSISTANT-EXAMINER: Chang; Daniel D.

ATTY-AGENT-FIRM: Morrison & Foerster LLP

ABSTRACT:

A programmable logic array integrated circuit is provided which comprises: a plurality of logic array blocks in which respective logic array blocks include, multiple respective programmable logic elements and respective random access memory arrays and corresponding memory access control circuitry and respective shared programmable local interfaces; and a network of conductors which is programmable to connect a respective local interface circuit of substantially any logic array block to a respective local interface of substantially any other logic array block.

33 Claims, 11 Drawing figures

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L5: Entry 20 of 25 File: USPT Mar 14, 2000

US-PAT-NO: 6038627
DOCUMENT-IDENTIFIER: US 6038627 A

TITLE: SRAM bus architecture and interconnect to an FPGA

DATE-ISSUED: March 14, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Plants; William C.	Santa Clara	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Actel Corporation	Sunnyvale	CA			02

APPL-NO: 09/ 039923 [PALM]
DATE FILED: March 16, 1998

INT-CL: [07] H03 K 19/177

US-CL-ISSUED: 710/126; 710/131, 326/37, 326/38, 326/39, 326/40, 365/185.01, 365/185.08, 365/185.11
US-CL-CURRENT: 710/100; 326/37, 326/38, 326/39, 326/40, 365/185.01, 365/185.08, 365/185.11

FIELD-OF-SEARCH: 710/126, 710/128, 710/129, 710/131, 326/37, 326/38, 326/39, 326/40, 326/41, 365/185.01, 365/185.08, 365/185.11

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4930097	May 1990	Ledenbach et al.	364/716
☐	5187392	February 1993	Allen	307/465
☐	5198705	March 1993	Galbraith et al.	307/465
☐	5208491	May 1993	Ebeling et al.	307/465
☐	5222066	June 1993	Grula et al.	371/21.1
☐	5744979	April 1998	Goetting	326/39
☐	5744980	April 1998	McGowan et al.	326/40
☐	5801547	September 1998	Kean	326/40
☐	5809281	September 1998	Steele et al.	711/170
☐	5815003	September 1998	Pedersen	326/39

☐	5815004	September 1998	Trimberger et al.	326/41
☐	5821776	October 1998	McGowan	326/41
☐	5825200	October 1998	Kolze	326/38
☐	5825201	October 1998	Kolze	326/39
☐	5825202	October 1998	Tavana et al.	326/39
☐	5825662	October 1998	Trimberger	364/491
☐	5828230	October 1998	Young	326/41
☐	5828538	October 1998	Apland et al.	361/56
☐	5831448	November 1998	Kean	326/41
☐	5835998	November 1998	Pedersen	326/40
☐	5838165	November 1998	Chatter	326/38
☐	5838167	November 1998	Erickson et al.	326/38
☐	5838584	November 1998	Kazarian	364/491
☐	5838892	November 1998	Wilson	714/799
☐	5838954	November 1998	Trimberger	395/500
☐	5847441	December 1998	Cutter et al.	257/530
☐	5847577	December 1998	Trimberger	326/38
☐	5848005	December 1998	Cliff et al.	365/230.03
☐	5850151	December 1998	Cliff et al.	326/39
☐	5850152	December 1998	Cliff et al.	326/40
☐	5850564	December 1998	Ting et al.	395/800.37
☐	5859542	January 1999	Pedersen	326/39
☐	5859543	January 1999	Kolze	326/41
☐	5859544	January 1999	Norman	326/40
☐	5861761	January 1999	Kean	326/41
☐	5869981	February 1999	Agrawal et al.	326/39
☐	5870586	February 1999	Baxter	395/500
☐	5880492	March 1999	Duong et al.	257/209
☐	5880512	March 1999	Gordon et al.	257/530
☐	5880597	March 1999	Lee	326/41
☐	5880598	March 1999	Duong	326/41
☐	5883526	March 1999	Reddy et al.	326/41
☐	5883850	March 1999	Lee et al.	365/230.03

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 415 542 A2	July 1990	EP	
0 889 593 A1	May 1995	EP	

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Etienne; Ario

ATTY-AGENT-FIRM: Schafer; Jonathan H.

ABSTRACT:

An SRAM bus architecture includes pass-through interconnect conductors. Each of the pass-through interconnect conductors is connected to routing channels of the general interconnect architecture of the FPGA through an element which includes a pass transistor connected in parallel with a tri-state buffer. The pass transistors and tri-state buffers are controlled by configuration SRAM bits. Some of the pass-through interconnect conductors are connected by programmable elements to the address, data and control signal lines of the SRAM blocks, while other pass through the SRAM blocks without being further connected to the SRAM bussing architecture.

3 Claims, 13 Drawing figures

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L5: Entry 21 of 25 File: USPT Feb 22, 2000

US-PAT-NO: 6028809
DOCUMENT-IDENTIFIER: US 6028809 A

TITLE: Programmable logic device incorporating a tristateable logic array block

DATE-ISSUED: February 22, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Schleicher; James	Sunnyvale	CA		
Lee; Andy	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Altera Corporation	San Jose	CA			02

APPL-NO: 09/ 100477 [PALM]
DATE FILED: June 19, 1998

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATION This application claims benefit of priority under 35 U.S.C. 119(e) of (i) U.S. Provisional application Ser. No. 60/050,327, filed Jun. 20, 1997 and entitled "TRI-STATE LOGIC ARRAY BLOCK FOR IMPLEMENTATION OF TRI-STATE BUSSES," and (ii) U.S. Provisional application Ser. No. 60/052,469, filed Jul. 14, 1997, and entitled "TRI-STATE LOGIC ARRAY BLOCK FOR IMPLEMENTATION OF TRISTATE BUSSES."

INT-CL: [07] G11 C 8/00

US-CL-ISSUED: 365/230.03; 365/230.08
US-CL-CURRENT: 365/230.03; 365/230.08

FIELD-OF-SEARCH: 365/230.03, 365/230.06

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4146749	March 1979	Pepping et al.	179/15
☐	5550782	August 1996	Cliff et al.	365/230.03

OTHER PUBLICATIONS

Bursky, Dave, "Combination RAM/PLD Opens New Application Options", Electronic Design, pp. 138-140, May 23, 1991.

Intel Corporation "10 ns Flexlogic FPGA with SRAM Option", Intel.sup..RTM., iFX780, pp. 2-24 2-46, Nov. 1993.
NGAI, Tony Kai-Kit, "An SRAM-Programmable Field-Reconfigurable Memory", Department of Electrical Engineering, University of Toronto, Thesis for Master of Applied Science, 1994.
Altera Corporation APEX 20K Programmable Logic Device Family, ALTERA.RTM., Oct. 1998, ver. 1.

ART-UNIT: 288

PRIMARY-EXAMINER: Nelms; David

ASSISTANT-EXAMINER: Tran; M.

ATTY-AGENT-FIRM: Beyer & Weaver, LLP

ABSTRACT:

The invention relates to an integrated circuit. The integrated circuit can be a programmable logic device that incorporates a multi-function block having a plurality of integrally connected function units where at least one of the function units within the multi-function block is a tristate logic unit. The programmable logic device also includes a tristate bus operatively connected to the tristate logic unit that can supply tristate logic signals to the tristate bus as well as receive tristate logic signals from the tristate bus. The tristate bus carries tristate data signals and address select signals that operate to select a desired one of the tristate logic units within the programmable logic device.

19 Claims, 9 Drawing figures

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L5: Entry 23 of 25 File: USPT Jan 25, 2000

US-PAT-NO: 6018490
DOCUMENT-IDENTIFIER: US 6018490 A
**** See image for Reexamination Certificate ****

TITLE: Programmable logic array integrated circuits

DATE-ISSUED: January 25, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cliff; Richard G.	Milpitas	CA		
Cope; L. Todd	San Jose	CA		
Mc Clintock; Cameron R.	Mountain View	CA		
Leong; William	San Francisco	CA		
Watson; James A.	Santa Clara	CA		
Huang; Joseph	San Jose	CA		
Ahanin; Bahram	Cupertino	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Altera Corporation	San Jose	CA			02

APPL-NO: 09/ 169332 [PALM]
DATE FILED: October 9, 1998

PARENT-CASE:
This application is a continuation of U.S. patent application Ser. No. 08/840,534, filed Apr. 22, 1997, now U.S. Pat. No. 5,838,628, which is a continuation of U.S. patent application Ser. No. 08/655,870, now U.S. Pat. No. 5,668,771, filed May 24, 1996, which is a continuation of U.S. patent application Ser. No. 08/245,509, now U.S. Pat. No. 5,550,782, filed May 18, 1994, which is a continuation-in-part of U.S. patent application Ser. No. 08/111,693, now U.S. Pat. No. 5,436,575, filed Aug. 25, 1993, which is a continuation-in-part of U.S. patent application Ser. No. 07/754,017, now U.S. Pat. No. 5,260,610, filed Sep. 3, 1991 and U.S. patent application Ser. No. 07/880,942, now U.S. Pat. No. 5,260,611, filed May 8, 1992, all the disclosures of which are incorporated by reference.

INT-CL: [06] G11 C 13/00

US-CL-ISSUED: 365/230.03; 365/189.02, 365/230.02
US-CL-CURRENT: 365/230.03; 365/189.02, 365/230.02

FIELD-OF-SEARCH: 365/189.01, 365/189.02, 365/189.05, 365/230.01, 365/230.03, 365/230.02

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	Re34444	November 1993	Kaplinsky	
☐	4293783	October 1981	Patil	
☐	4642487	February 1987	Carter	307/465
☐	4706216	November 1987	Carter	365/94
☐	4758985	July 1988	Carter	365/94
☐	4825414	April 1989	Kawata	
☐	4831591	May 1989	Imazeki et al.	
☐	4855958	August 1989	Ikeda	
☐	4870302	September 1989	Freeman	307/465
☐	4903236	February 1990	Nakayama et al.	365/189.04
☐	4963770	October 1990	Keida	
☐	4975601	December 1990	Steele	
☐	5042004	August 1991	Agrawal et al.	
☐	5089993	February 1992	Neal et al.	365/230.08
☐	5099150	March 1992	Steele	
☐	5122685	June 1992	Chan et al.	
☐	5128559	July 1992	Steele	307/465
☐	5138577	August 1992	Oh	365/189.05
☐	5144582	September 1992	Steele	
☐	5258668	November 1993	Cliff et al.	307/465
☐	5260610	November 1993	Pedersen et al.	307/465
☐	5260611	November 1993	Cliff	307/465
☐	5291444	March 1994	Scott	365/189.05
☐	5313119	May 1994	Cooke et al.	
☐	5315178	May 1994	Snider	
☐	5329460	July 1994	Agrawal et al.	
☐	5336950	August 1994	Popli et al.	
☐	5343406	August 1994	Freeman et al.	
☐	5349250	September 1994	New	307/465
☐	5352940	October 1994	Watson	
☐	5408434	April 1995	Stansfield	
☐	5414377	May 1995	Freidin	
☐	5425036	June 1995	Liu et al.	371/23
☐	5426378	June 1995	Ong	
☐	5436575	July 1995	Pedersen et al.	
☐	5448522	September 1995	Huang	365/189.04
☐	5471425	November 1995	Yumitori et al.	
☐	5550782	August 1996	Cliff et al.	
	5566123	October 1996	Freidin et al.	365/230.05

☐			
☐	5809281	September 1998	Steele et al.
☐	5835405	November 1998	Tsui et al.

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0081917	August 1983	EP	
0410759 A2	January 1991	EP	
0415542 A2	March 1991	EP	
0420389 A1	April 1991	EP	
0507507 A2	October 1992	EP	
0530985 A2	March 1993	EP	
0569137 A2	November 1993	EP	
01091525	April 1989	JP	
01091526	April 1989	JP	
WO 94/10754	May 1994	WO	
WO 95/16993	June 1995	WO	

OTHER PUBLICATIONS

Xilinix, The Programmable Logic Data Book, 1993.
Masumoto, Rodney T., "Configurable On-Chip RAM Incorporated into High Speed Logic Array," IEEE Custom Integrated Circuits Conference, Jun. 1985, CH2157-6/85/0000-0240, pp. 240-243.
Landry, Steve, "Application -Specific ICs, Relying on RAM, Implement Almost Any Logic Function," Electronic Design, Oct. 31, 1985, pp. 123-130.
Bursky, Dave, "Shrink Systems with One-Chip Decoder, EPROM, and RAM," Electronic Design, Jul. 28, 1988, pp. 91-94.
Kawana, Keiichi et al., "An Efficient Logic Block Interconnect Architecture for User-Reprogrammable Gate Array," IEEE 1990 Custom Integrated Circuits Conf., May 1990, CH2860-5/90/0000-0164, pp. 31.3.1 to 31.3.4.
Shubat, Alexander et al., "A Family of User-Programmable Peripherals with a Functional Unit Architecture," IEEE Jor. of Solid-State Circuits, vol. 27, No. 4, Apr. 1992, 0018-9200/92 $03.00, pp. 515-529.
"AT&T's Orthogonal ORCA Targets the FPGA Future," 8029 Electronic Engineering, 64, No. 786, Jun. 1992, pp. 9-10.
Bursky, Dave, "FPGA Advances Cut Delays, Add Flexibility," 2328 Electronic Design, 40, No. 20, Oct. 1, 1992, pp. 35-43.
Smith, Daniel, "Intel's FLEXlogic FPGA Architecture," IEEE 1063-6390/93, 1993 pp. 378-384.
Bursky, Dave, "Denser, Faster FPGAs Vie for Gate-Array Applications," 2328 Electronic Design, 41, No. 11, May 27, 1993, pp. 55-75.
Ngai, Kai-Kit Tony, "An SRAM-Programmable Field-Reconfigurable Memory," Presentation at University of Toronto, Canada, Jun. 1993, pp. 1-14.
Kautz, "Cellular Logic in Memory Arrays," IEEE Trans. on Computers, vol. C-18, No. 8, Aug. 1969, pp. 719-727.
Stone, "A Logic in Memory Computer," IEEE Trans. on Computers, Jan. 1970, pp. 73-78.
Manning, "An Approach to Highly Integrated Computer Maintained Cellular Arrays," IEEE Trans. on Computers, vol. C-26, No. 6, Jun. 1977,pp. 536-552.
Patil et al., "A Programmable Logic Approach for VLSI," IEEE Trans. on Computers, vol. C-28, No. 9, Sep. 1979, pp. 594-601.
Seitz, "Concurrent VLSI Architectures," IEEE Trans. on Computers, vol. C-33, No. 12, Dec. 1984, pp. 1247-1265.
Hsieh et al., "Third Generation Architecture Boosts Speed and Density of Field Programmable Gate Arrays," Proc. of IEEE CICC Conf., May 1990, pp. 31.2.1 to 31.2.7.
Bursky, "Combination RAM/PLD Opens New Application Options," Electronic Design, May 23, 1991, pp. 138-140.
Ling et al., "WASMII: A Data Driven Computer on a Virtual Hardware," Proc. of IEEE Field Prog.

Custom Computing Machines Conf., Napa, California, Apr. 1993, pp. 33-42.
Casselman, "Virtual Computing and The Virtual Computer," Jul. 1993, p. 43.
Quenot et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Proc. of IEEE FCCM Conf., Napa, California, Feb. 1994, pp. 91-100.
Plus Logic "FPSL5110 Intelligent Data Buffer" Product Brief, Plus Logic, Inc., San Jose, California, Oct. 1990, pp. 1-6.
Larsson, T, "Programmable Logic Circuits: The Luxury Alternatives are Coming Soon," Elteknik-med-Aktuell Electronik, No. 4, Feb. 25-Mar. 9, 1988, pp. 37-38, (with English abstract).
Intel Preliminary Datasheet, "iFX780: 10ns FLEXlogic FPGA wuth SRAM Option," Nov. 1993, pp. 2-24 to 2-46.
Quinnell, Richard A., "FPGA Family Offers Speed, Density, On-Chip RAM, and WIDE-Decode Logic," EDN Dec. 6, 1990, pp. 62-63.
Satoh, Hisayasu et al., "A 209K-Transistor ECL Gate Array with RAM," IEEE Jor. of Solid-State Ciruits, vol. 24, No. 5, Oct. 1989, pp. 1275-1279.
"Optimized reconfigurable cell array (ORCA) series field-programmable gate arrays," AT&T Microelectronics, pp. 1-87 (Advance Data Sheet, Feb. 1985).
"The Programmable Logic Data Book," Xilinx, Inc., 1994, pp. 2-5-2-102.

ART-UNIT: 288

PRIMARY-EXAMINER: Fears; Terrell W.

ATTY-AGENT-FIRM: Townsend and Townsend and Crew LLP

ABSTRACT:

A programmable logic array integrated circuit has a number of programmable logic modules which are grouped together in a plurality of logic array blocks ("LABs"). The LABs are arranged on the circuit in a two dimensional array. A conductor network is provided for interconnecting any logic module with any other logic module. In addition, adjacent or nearby logic modules are connectable to one another for such special purposes as providing a carry chain between logic modules and/or for connecting two or more modules together to provide more complex logic functions without having to make use of the general interconnection network. Another network of so-called fast or universal conductors is provided for distributing widely used logic signals such as clock and clear signals throughout the circuit. Multiplexers can be used in various ways to reduce the number of programmable interconnections required between signal conductors.

36 Claims, 33 Drawing figures

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Search Results - Record(s) 1 through 10 of 15 returned.

☐ 1. Document ID: US 20040199689 A1

L8: Entry 1 of 15 File: PGPB Oct 7, 2004

PGPUB-DOCUMENT-NUMBER: 20040199689
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040199689 A1

TITLE: SRAM bus architecture and interconnect to an FPGA

PUBLICATION-DATE: October 7, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Plants, William C.	Santa Clara	CA	US	

US-CL-CURRENT: 710/100

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 20030151426 A1

L8: Entry 2 of 15 File: PGPB Aug 14, 2003

PGPUB-DOCUMENT-NUMBER: 20030151426
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030151426 A1

TITLE: Logic circuits using polycrystalline semiconductor thin film transistors

PUBLICATION-DATE: August 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Islam, Mujahid	Cambridge		GB	

US-CL-CURRENT: 326/37

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 6799240 B1

L8: Entry 3 of 15 File: USPT Sep 28, 2004

US-PAT-NO: 6799240
DOCUMENT-IDENTIFIER: US 6799240 B1

TITLE: SRAM bus architecture and interconnect to an FPGA

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 4. Document ID: US 6759870 B2

L8: Entry 4 of 15 File: USPT Jul 6, 2004

US-PAT-NO: 6759870
DOCUMENT-IDENTIFIER: US 6759870 B2

TITLE: Programmable logic array integrated circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 6404225 B1

L8: Entry 5 of 15 File: USPT Jun 11, 2002

US-PAT-NO: 6404225
DOCUMENT-IDENTIFIER: US 6404225 B1

TITLE: Integrated circuit incorporating a programmable cross-bar switch

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6326807 B1

L8: Entry 6 of 15 File: USPT Dec 4, 2001

US-PAT-NO: 6326807
DOCUMENT-IDENTIFIER: US 6326807 B1

TITLE: Programmable logic architecture incorporating a content addressable embedded array block

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 6292017 B1

L8: Entry 7 of 15 File: USPT Sep 18, 2001

US-PAT-NO: 6292017
DOCUMENT-IDENTIFIER: US 6292017 B1

TITLE: Programmable logic device incorporating function blocks operable as wide-shallow RAM

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 6249143 B1

L8: Entry 8 of 15 File: USPT Jun 19, 2001

US-PAT-NO: 6249143
DOCUMENT-IDENTIFIER: US 6249143 B1

TITLE: Programmable logic array integrated circuit with distributed random access memory array

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 9. Document ID: US 6195788 B1

L8: Entry 9 of 15 File: USPT Feb 27, 2001

US-PAT-NO: 6195788
DOCUMENT-IDENTIFIER: US 6195788 B1

TITLE: Mapping heterogeneous logic elements in a programmable logic device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 10. Document ID: US 6181159 B1

L8: Entry 10 of 15 File: USPT Jan 30, 2001

US-PAT-NO: 6181159
DOCUMENT-IDENTIFIER: US 6181159 B1

TITLE: Integrated circuit incorporating a programmable cross-bar switch

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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Terms	Documents
L5 and L7	15

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Search Results - Record(s) 11 through 15 of 15 returned.

☐ 11. Document ID: US 6160419 A

L8: Entry 11 of 15 File: USPT Dec 12, 2000

US-PAT-NO: 6160419
DOCUMENT-IDENTIFIER: US 6160419 A

TITLE: Programmable logic architecture incorporating a content addressable embedded array block

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 12. Document ID: US 6104208 A

L8: Entry 12 of 15 File: USPT Aug 15, 2000

US-PAT-NO: 6104208
DOCUMENT-IDENTIFIER: US 6104208 A

TITLE: Programmable logic device incorporating function blocks operable as wide-shallow RAM

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 13. Document ID: US 6057707 A

L8: Entry 13 of 15 File: USPT May 2, 2000

US-PAT-NO: 6057707
DOCUMENT-IDENTIFIER: US 6057707 A

TITLE: Programmable logic device incorporating a memory efficient interconnection device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 14. Document ID: US 6038627 A

L8: Entry 14 of 15 File: USPT Mar 14, 2000

US-PAT-NO: 6038627
DOCUMENT-IDENTIFIER: US 6038627 A

TITLE: SRAM bus architecture and interconnect to an FPGA

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

· ☐ ·15. Document ID: US 5670897 A

L8: Entry 15 of 15 File: USPT Sep 23, 1997

US-PAT-NO: 5670897
DOCUMENT-IDENTIFIER: US 5670897 A

TITLE: High speed mask register for a configurable cellular array

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L5 and L7	15

Display Format: - Change Format

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US006799240B1

(12) **United States Patent**
Plants

(10) **Patent No.: US 6,799,240 B1**
(45) **Date of Patent: Sep. 28, 2004**

(54) **SRAM BUS ARCHITECTURE AND INTERCONNECT TO AN FPGA**

(75) Inventor: William C. Plants, Santa Clara, CA (US)

(73) Assignee: Actel Corporation, Mountain View, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/406,860

(22) Filed: Apr. 4, 2003

Related U.S. Application Data

(63) Continuation of application No. 10/247,114, filed on Sep. 18, 2002, which is a continuation of application No. 09/512,133, filed on Feb. 23, 2000, now Pat. No. 6,496,887, which is a continuation of application No. 09/039,923, filed on Mar. 16, 1998, now Pat. No. 6,038,627.

(51) Int. Cl.[7] G06F 13/00
(52) U.S. Cl. 710/305; 710/100; 716/16
(58) Field of Search 710/100, 305, 710/316, 300, 313; 326/37-39; 365/185.01, 185.11; 711/104; 716/16

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,277,844	A	7/1981	Hancock et al.	371/38
4,758,745	A	7/1988	Elgamal et al.	307/465
4,930,097	A	5/1990	Ledenbach et al.	364/716
5,187,392	A	2/1993	Allen	307/465
5,208,491	A	5/1993	Ebeling et al.	307/465
5,222,066	A	6/1993	Gruia et al.	371/21.1
5,365,485	A	11/1994	Ward et al.	365/221
5,375,089	A	12/1994	Lo	365/189.04
5,611,042	A	3/1997	Lordi	395/182.04
5,744,979	A	4/1998	Goetting	326/39
5,744,980	A	4/1998	McGowan et al.	326/40
5,761,140	A	6/1998	Choi	365/201
5,802,547	A	9/1998	Kean	326/40
5,809,281	A	9/1998	Steele et al.	325/497.01
5,815,003	A	9/1998	Pedersen	326/39
5,815,004	A	9/1998	Trimberger et al.	326/41
5,821,776	A	10/1998	McGowan	326/41
5,825,200	A	10/1998	Kolze	326/38
5,825,201	A	10/1998	Kolze	326/39
5,825,202	A	10/1998	Tavana et al.	329/39
5,825,662	A	10/1998	Trimberger	364/491
5,825,838	A	10/1998	Park et al.	364/56
5,828,230	A	10/1998	Young	364/41
5,831,448	A	11/1998	Kean	326/41
5,835,157	A	11/1998	Bouguerra et al.	326/38
5,835,998	A	11/1998	Pedersen	326/40
5,838,584	A	11/1998	Kazarian	364/491

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP	0 415 542 A3	3/1991	H03K/19/173
EP	0 415 542 A2	3/1991	H03K/19/173
EP	0 869 593 A1	1/1999	H03K/19/173

OTHER PUBLICATIONS

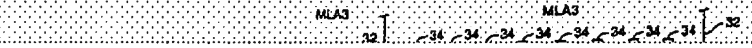
"An analytical delay model for SRAM-based FPGA interconnections" by Zuon Feng, Huang Zhijun, Tong Jiarong and Tang Pushan (abstract only).*

Primary Examiner—Gopal C. Ray
(74) *Attorney, Agent, or Firm*—Sierra Patent Group, Ltd.

(57) **ABSTRACT**

An SRAM bus architecture includes pass-through interconnect conductors. Each of the pass-through interconnect conductors is connected to routing channels of the general interconnect architecture of the FPGA through an element which includes a pass transistor connected in parallel with a tri-state buffer. The pass transistors and tri-state buffers are controlled by configuration SRAM bits. Some of the pass-through interconnect conductors are connected by programmable elements to the address, data and control signal lines of the SRAM blocks, while other pass through the SRAM blocks with out being further connected to the SRAM bussing architecture.

3 Claims, 6 Drawing Sheets



US006462578B2

(12) **United States Patent**
Ting

(10) **Patent No.: US 6,462,578 B2**
(45) **Date of Patent: *Oct. 8, 2002**

(54) **ARCHITECTURE AND INTERCONNECT SCHEME FOR PROGRAMMABLE LOGIC CIRCUITS**

(75) Inventor: **Benjamin S. Ting**, Saratoga, CA (US)

(73) Assignee: **BTR, Inc.**, Reno, NV (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/482,149**

(22) Filed: **Jan. 12, 2000**

(65) **Prior Publication Data**

US 2002/0101258 A1 Aug. 1, 2002

Related U.S. Application Data

(63) Continuation of application No. 08/909,928, filed on Aug. 11, 1997, which is a continuation of application No. 08/534,500, filed on Sep. 27, 1995, which is a continuation of application No. 08/229,923, filed on Apr. 19, 1994, which is a continuation-in-part of application No. 08/101,197, filed on Aug. 3, 1993, now Pat. No. 5,457,410.

(51) **Int. Cl.**[7] **H03K 19/177**

(52) **U.S. Cl.** **326/41**; 326/39

(58) **Field of Search** 326/38, 39, 40, 326/41

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,020,469 A 4/1977 Manning 326/40

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP 0435542 7/1991

OTHER PUBLICATIONS

Minnick, R.C. "A Survey of Microcellular Research," Journal of the Association for Computing Machinery, vol. 14, No. 2, Apr. 1967, pp. 203–241.

(List continued on next page.)

Primary Examiner—Michael Tokar
Assistant Examiner—Vibol Tan
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman, LLP

(57) **ABSTRACT**

An architecture and distributed hierarchical interconnect scheme for field programmable gate arrays (FPGAs). The FPGA is comprised of a number of cells which perform logical functions on input signals. Programmable interconnections provide connectability between each output of a cell belonging to a logical cluster to at least one input of each of the other cells belonging to that logical cluster. A set of programmable block connectors are used to provide connectability between logical clusters of cells and accessibility to the hierarchical routing network. An uniformly distributed first layer of routing network lines is used to provide connections amongst sets of block connectors. An uniformly distributed second layer of routing network lines is implemented to provide connectability between different first layers of routing network lines. Switching networks are used to provide connectability between the block connectors and routing network lines corresponding to the first layer. Other switching networks provide connectability between the routing network lines corresponding to the first layer to routing network lines corresponding to the second layer. Additional uniformly distributed layers of routing network lines are implemented to provide connectability between different prior layers of routing network lines. An additional routing layer is added when the number of cells is increased as a square function of two of the prior cell count in the array while the length of the routing lines and the number of routing lines increases as a linear function of two. Programmable bidirectional passgates are used as switches to control which of the routing network lines are to be connected.

US006134173A

United States Patent [19]

Cliff et al.

[11] Patent Number: 6,134,173

[45] Date of Patent: Oct. 17, 2000

[54] **PROGRAMMABLE LOGIC ARRAY INTEGRATED CIRCUITS**

[75] Inventors: **Richard G. Cliff**, Milpitas; **L. Todd Cope**, San Jose; **Cameron R. McClintock**, Mountain View; **William Leong**, San Francisco; **James A. Watson**, Santa Clara; **Joseph Huang**, San Jose; **Bahram Ahanin**, Cupertino, all of Calif.

[73] Assignee: **Altera Corporation**, San Jose, Calif.

[21] Appl. No.: 09/184,383

[22] Filed: Nov. 2, 1998

Related U.S. Application Data

[63] Continuation of application No. 08/851,862, May 6, 1997, which is a continuation of application No. 08/655,870, May 24, 1996, Pat. No. 5,668,771, which is a continuation of application No. 08/245,509, May 18, 1994, Pat. No. 5,550,782, which is a continuation-in-part of application No. 08/111,593, Aug. 25, 1993, Pat. No. 5,436,575, which is a continuation-in-part of application No. 07/754,017, Sep. 3, 1991, Pat. No. 5,260,610, which is a continuation-in-part of application No. 07/880,942, May 8, 1992, Pat. No. 5,260,611.

[51] Int. Cl.[7] G11C 13/00

[52] U.S. Cl. 365/230.03; 365/189.02

[58] Field of Search 365/189.01, 189.02, 365/189.05, 230.01, 230.03, 230.02, 77

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 34,444	11/1993	Kaplinsky	
4,293,783	10/1981	Patil	

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

0081917	8/1983	European Pat. Off.
0410759 A2	1/1991	European Pat. Off.
0415542 A2	3/1991	European Pat. Off.
0507507 A2	10/1992	European Pat. Off.
0530985 A2	3/1993	European Pat. Off.
0569137 A2	11/1993	European Pat. Off.
01091525	4/1989	Japan
01091526	4/1989	Japan
WO 94/10754	5/1994	WIPO
WO 95/16993	6/1995	WIPO

OTHER PUBLICATIONS

"Optimized Reconfigurable Cell Arry (ORCA) Series Field-Programmable Gate Arrays," AT&T Microelectronics, pp. 1–67, Advance Data Sheet, Feb. 1985.

"The Programmable Logic Data Book," Xilinx, Inc., 1994, pp. 2–5 to 2–102.

Masumoto, Rodney T., "Configurable On-Chip RAM Incorporated into High Speed Logic Array," IEEE Custom Integrated Circuits Conference, Jun. 1985, CH2157–6/85/0000–0240, pp. 240–243.

(List continued on next page.)

Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Townsend and Townsend and Crew LLP

[57] **ABSTRACT**

A programmable logic array integrated circuit has a number of programmable logic modules which are grouped together in a plurality of logic array blocks ("LABs"). The LABs are arranged on the circuit in a two dimensional array. A conductor network is provided for interconnecting any logic module with any other logic module. In addition, adjacent or nearby logic modules are connectable to one another for such special purposes as providing a carry chain between logic modules and/or for connecting two or more modules together to provide more complex logic functions without having to make use of the general interconnection network. Another network of so-called fast or universal conductors is provided for distributing widely used logic signals such as clock and clear signals throughout the circuit. Multiplexers can be used in various ways to reduce the number of programmable interconnections required between signal conductors.

148 Claims, 28 Drawing Sheets